REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 19, 2004. Upon entry of the amendments in this response, claims 1 - 24 remain pending. In particular, Applicants have amended claims 1 –3, 10 – 14 and 19 – 24. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

In the Drawings

The Office Action indicates that Applicants are required to furnish formal drawings in response to this office action. Applicants submit herewith copies of the originally filed formal drawings.

Rejections Under 35 U.S.C. §103

The Office Action indicates that claims 1 - 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Siegel*. Applicants respectfully traverse the rejection for at least the reasons indicated below.

In this regard, the Office Action indicates that *Siegel* does not disclose the use of modifying a value contained in the first register in response to a transfer of a data unit into the buffer or modifying a value contained in the register in response to a transfer of a data unit out of the buffer. Applicants respectfully agree with this contention. However, the Office Action alleges that:

> *Siegel* discloses the use of incrementing the next address corresponding to the data area in cache memory in which the next block of data is to be stored and that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement *Siegel's* system by modifying the value contained in the register. Such an implementation would allow *Siegel's* system an enhanced capability of eliminating the breaks and presenting data to the host computer caused by delays associated with locating a particular data block (Office Action at p. 3).

Applicant respectfully disagrees with the above-mentioned contention of the Office Action for several reasons. First, it appears that the Office Action has taken some form of Official Notice that modifying a value to eliminate breaks in presenting data to a host computer caused by delays associated with locating a particular data block is so notoriously well known that no specific teaching need to presented to the Applicant in the Office Action. However, Applicants respectfully assert that such a teaching is not notoriously well known and respectfully requests the Examiner to provide evidence of such teaching in a subsequent Office Action. Second, Applicants respectfully assert that there is no motivation to modify the teachings of *Siegel* in the manner suggested for the purpose of attempting to present a prima facie case of obviousness. Lacking such a proper motivation, Applicants respectfully assert that the rejection is legally deficient. Third, even if such motivation does exist, Applicants respectfully assert that modifying *Siegel* in the manner presented in the Office Action still does not appear to present a prima facie case of obviousness. That is, the Office Action seems to miscorrelate the concept of incrementing the next address corresponding to the data area with modifying a value contained in the register for tracking a number of data units that have been transferred into and out of the buffer. Therefore, even if the alleged teachings presented in the Office Action are notoriously well known and the motivation to combine such teachings with *Siegel* is proper, the resultant combination still does not teach or reasonably suggest all the features/limitations recited in Applicants' claims.

Additionally, it appears that the Office Action has attributed various structure and/or functionality to *Siegel* that is neither expressly taught nor apparent in the teachings of *Siegel*. Specifically, as will be discussed in detail later, the Office Action alleges that *Siegel* teaches various registers such as Applicant's recited fourth through eighth registers. However, upon review of Siegel, it appears that *Siegel* only teaches (1) a base count register, (2) a base address register, and (3) a data count register. Therefore, if the rejections of claims reciting

more than three registers are to be maintained, Applicants respectfully request clarification of the teachings of *Siegel* relied upon for such rejections so that Applicants have an adequate opportunity to respond.

Turning now to the claims, claim 1 recites:

> 1. A method for transferring data between a host device and a storage medium, comprising:
> receiving from the host device a command to transfer data between the host device and the storage medium;
> ***storing in a first register a value*** for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out of the buffer;
> ***modifying the value contained in the first register in response to a transfer of a data unit into the buffer; and***
> ***modifying the value contained in the first register in response to a transfer of a data unit out of the buffer.***
> (Emphasis Added).

Applicants respectfully assert that the cited references, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 1. Specifically, Applicants respectfully assert that the cited art does not teach or reasonably suggest at least the features/limitations emphasized above in claim 1. Therefore, Applicants respectfully assert that claim 1 is in condition for allowance. Since claims 2-9 incorporate all the features/limitations of claim 1, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability. By way of example, claim 2 recites:

> 2. The method of claim 1, further comprising:
> storing in a second register a value for incrementing the value contained in the first register; and
> incrementing the value contained in the first register by the value contained in the second register.

Applicants respectfully assert that the cited art, either individually or in combination, does not teach or reasonably suggest at least the additional features/limitations recited above

in claim 2. Therefore, Applicants respectfully assert that at least claim 2 is in condition for allowance.

As another example, Claim 3 recites:

> 3. The method of claim 1, further comprising:
> storing in a third register a value for decrementing the value contained in the first register; and
> decrementing the value contained in the first register by the value contained in the third register.

Applicants also respectfully assert that the cited art, either individually or in combination, does not teach or reasonably suggest at least the additional features/limitations recited above in claim 3. Therefore, Applicants respectfully assert that at least claim 3 is in condition for allowance.

As yet another example, claim 6 recites:

> 6. The method of claim 5, further comprising:
> storing in an eighth register a value representing a storage capacity of the buffer.

Applicants respectfully assert that the cited art, either individually or in combination, does not teach or reasonably suggest at least the additional features/limitations recited above in claim 6. Therefore, Applicants respectfully assert that at least claim 6 is in condition for allowance.

Referring now to claim 10, that claim recites:

> 10. A data transfer system for transferring data between a host device and a storage medium, comprising:
> a host interface that receives from the host device a command to transfer data between the host device and the storage medium;
> a buffer that temporarily stores data that is transferred between the host device and the storage medium;
> ***a first register that stores a value*** for tracking a number of data units that have been transferred into the buffer but that have not yet been transferred out of the buffer;
> ***a second register that stores a value for incrementing the value contained in the first register; and***

a third register that stores a value for decrementing the value contained in the first register.
(Emphasis Added).

Applicants respectfully assert that the cited references, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 10. Specifically, Applicants respectfully assert that the cited art does not teach or reasonably suggest at least the features/limitations emphasized above in claim 10. Therefore, Applicants respectfully assert that claim 10 is in condition for allowance. Since claims 11-18 incorporate all the features/limitations of claim 10, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

With regard to claim 19, that claim recites:

19. A method for transferring data between a host device and a storage medium, comprising:
receiving from the host device a command to transfer data between the host device and the storage medium;
storing in a first register a value for determining a buffer's fullness;
incrementing the value contained in the first register by a value contained in a second register; and
decrementing the value contained in the first register by a value contained in a third register.
(Emphasis Added).

Applicants respectfully assert that the cited references, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 19. Specifically, Applicants respectfully assert that the cited art does not teach or reasonably suggest at least the features/limitations emphasized above in claim 19. Therefore, Applicants respectfully assert that claim 19 is in condition for allowance. Since claims 20-21 incorporate all the features/limitations of claim 19, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

With respect to claim 22, that claim recites:

> 22. An application specific integrated circuit (ASIC) for transferring data between a host device and a storage medium, comprising:
> a buffer that temporarily stores data that is transferred between the host device and the storage medium;
> ***a first register that stores a value*** for determining the buffer's fullness;
> ***a second register that stores a value for incrementing the value contained in the first register; and***
> ***a third register that stores a value for decrementing the value contained in the first register.***
> (Emphasis Added).

Applicants respectfully assert that the cited references, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 22. Specifically, Applicants respectfully assert that the cited art does not teach or reasonably suggest at least the features/limitations emphasized above in claim 22. Therefore, Applicants respectfully assert that claim 1 is in condition for allowance. Since claims 23-24 incorporate all the features/limitations of claim 22, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

Cited Art Made of Record

The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1 - 24 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450,
on 8/25/04.

Stephanie Riley
Signature